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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,004	10/28/2003	Lyle E. Adams	63479.0116	4256

23309 7590 11/17/2005

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,004	ADAMS ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

Claims 6-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In each of multiple dependent claims 6-9, line 1, "A dependent claim" is unclear because they are not properly directed to a statutory category. Since claims 1-5 are directed to different statutory categories, it is suggested that, instead of using multiple dependent claim, a set of dependent claims is provided under its independent claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Elabd (6,526,462).

As broadly drafted, these claims do not define any structure/step that differs from Elabd.

With regard to claim 1, Elabd discloses a System-on-Chip (SOC) interconnection apparatus (shown generally at Fig. 2), comprising: a single semiconductor integrated circuit (SOC, Fig. 2, for example) that includes one or more requestors (CPU 4 or DSP 2, for example) and one or more addressable targets (32/34, for example), wherein each said addressable target (32/34, for example) has a unique address space (one of the ten addresses of the memory space 86, see at least col. 11, line 35 to col. 12, line 7) and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system (the addressable targets can be an internal or external memory 32/34); an internal switching

fabric (the routing/switching RCPU and dedicated memory buses 25a-25n constitute internal switching fabric) that that routes signals between said requesters and said addressable targets, said internal switching fabric further comprises one or more decoder/router elements (memory bus 25a-25n decodes the address of at least one addressable target, see at least col. 6, lines 15-17, and claim 17), wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map (memory mapping, see at least col. 11, line 35 to col. 12, line 7), and routes said request to said designated target (the routing/switching RCPU routes the request to a designated target); one or more requestor connection ports, wherein each said connection port connects one of said requesters to said internal switching fabric; and one or more target connection ports, wherein each said target port connects one of said addressable targets to said internal switching fabric (it is clearly inherent that there are connection ports, since it is clear that dedicated memory buses 25a-25n and MT MMS having RCPU provides communications and connections between the masters and the targets).

With regard to claim 2, Elabd discloses a system (see col. 1, lines 23-59) that includes a System-on-Chip (SOC) having an interconnection apparatus (shown generally at Fig. 2) comprising: a single semiconductor integrated circuit (SOC, Fig. 2, for example) that includes one or more requesters (CPU 4 or DSP 2, for example) and one or more addressable targets (32/34, for example), wherein each said addressable target has a unique address space (one of the ten addresses of the memory space 86,

see at least col. 11, line 35 to col. 12, line 7) and further comprises one or more of the following: resident memory, a memory controller for resident or off-chip memory, an addressable bridge to a device, an addressable bridge to a system, or an addressable bridge to a sub-system (the addressable targets can be an internal or external memory 32/34); an internal switching fabric (the routing/switching RCPY and dedicated memory buses 25a-25n constitute internal switching fabric) that routes signals between said requestors and said addressable targets, said internal switching fabric further comprises one or more decoder/router elements (memory bus 25a-25n decodes the address of at least one addressable target, see at least col. 6, lines 15-17, and claim 17), wherein each decoder/router element receives a request from a requestor, determines which said addressable target is the designated target using an internal system memory map, and routes said request to said designated target (the routing/switching RCPU routes the request to a designated target); one or more requestor connection ports, wherein each said connection port connects one of said requesters to said internal switching fabric; and one or more target connection ports, wherein each said target port connects one of said addressable targets to said internal switching fabric (it is clearly inherent that there are connection ports, since it is clear that dedicated memory buses 25a-25n and MT MMS having RCPU provides communications and connections between the masters and the targets).

With regard to claims 3 and 4, see discussion above regarding claims 1 and 2.

With regard to claim 5, see discussion above regarding claims 1 and 2. Note also that any operation performed by software can also be built directly into the hardware and any instruction executed by the hardware can also be simulated in software.

With regard to claim 6, it is clear that the internal switching fabric includes at least the arbiter 52.

With regard to claim 7, it is clear that one of said one or more decoder/router elements further comprises one of the following: a decoder/router element that routes requests to all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for all of said one or more addressable targets; or a decoder/router element that routes requests to less than all of said one or more addressable targets using an internal system memory map that includes unique address space information for less than all of said one or more addressable targets (see Fig. 4 and description thereof, see also at least col. 11, line 35 to col. 12, line 7.

With regard to claims 8 and 9, it is clear that independently accessible requestor port and an independently accessible target port are provided in Elabd for a plurality of individual masters and individual targets.

With regard to claim 10, see discussion above. See also Figs. 4, 6 (a,b) and 12C, and description thereof. Note that MT MMS has the state machines.

With regard to claims 11-15, see discussion above regarding claims 1-12.

U.S. Patent Nos. 6,769,046 to Adams et al., 6,353,867 to Qureshi et al., 6,601,126 to Zaidi et al., 6,262,594 to Cheung et al., 6,874,039 to Ganapathy et al., 5,935,232 to Lambreht, US Patent Pub. Nos. 2005/0071533 to Adams et al., 2003/0163798 to Hwang et al., The IBM CoreConnect Bus Architecture, SiliconBackplane III MicroNetwork IP, System-on-a Chip Bus Architecture for Embedded Applications, OpenCores SOC Bus Review, Viper: A Multiprocessor SOC for Advanced Set-Top Box and Digital TV Systems, and New IP Integration Strategies Simplify SOC Design are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang
Primary Exam